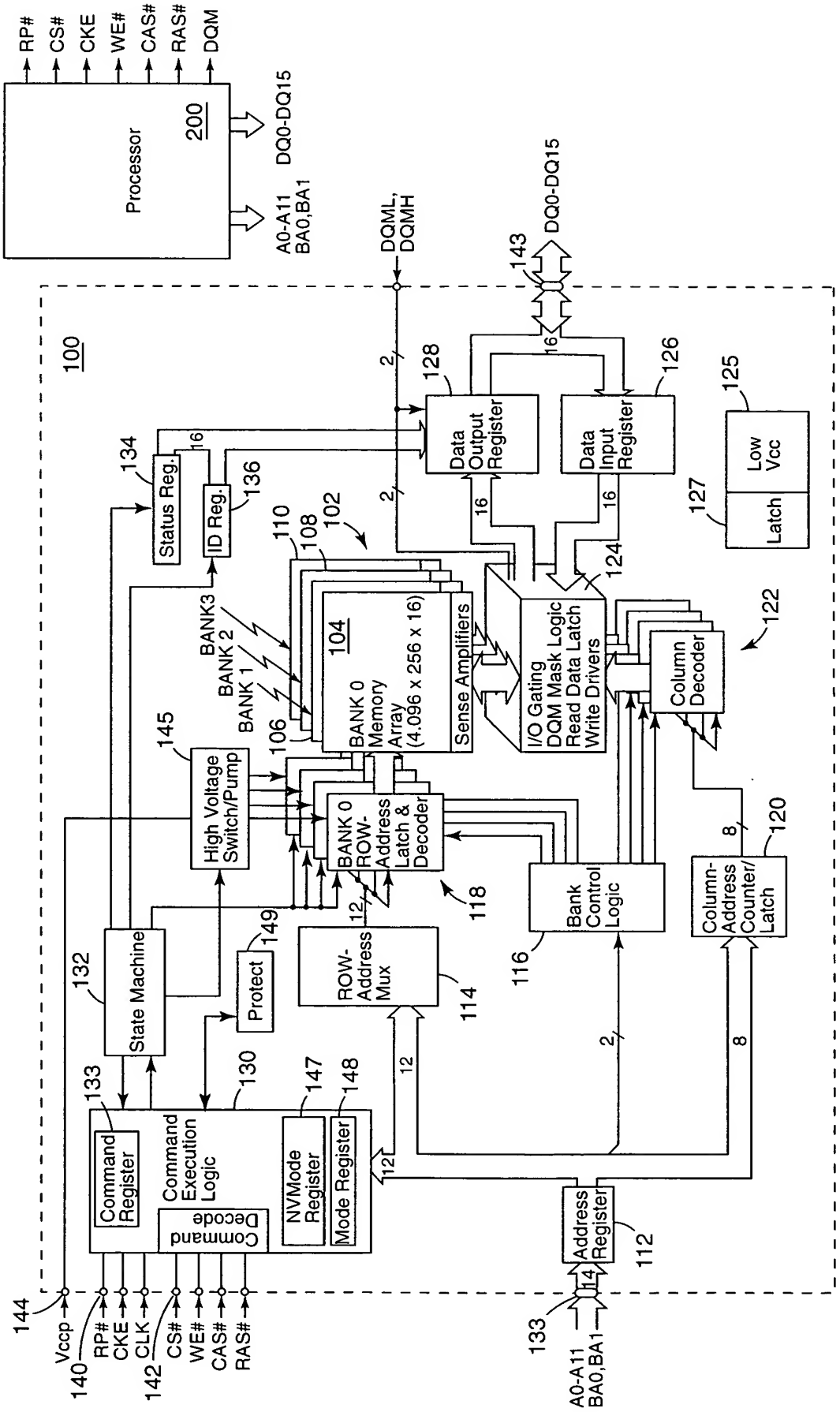

RP#
CS#
CKE
WE#
CAS#
RAS#
DQM
Processor
200
DQ0-DQ15
A0-A11
BA0,BA1
DQML,
DQMH
143
100
Data Output Register
Data Input Register
Low Vcc
Latch
Status Reg.
ID Reg.
BANK3
BANK 2
BANK 1
BANK 0 Memory Array (4,096 x 256 x 16)
Sense Amplifiers
I/O Gating DQM Mask Logic Read Data Latch Write Drivers
Column Decoder
High Voltage Switch/Pump
BANK 0 ROW-Address Latch & Decoder
Bank Control Logic
Column-Address Counter/ Latch
State Machine
Protect
ROW-Address Mux
Command Register
Command Execution Logic
Command Decode
NVMode Register
Mode Register
Address Register
Vccp
RP#
CKE
CLK
CS#
WE#
CAS#
RAS#
A0-A11
BA0,BA1

Fig. 1A

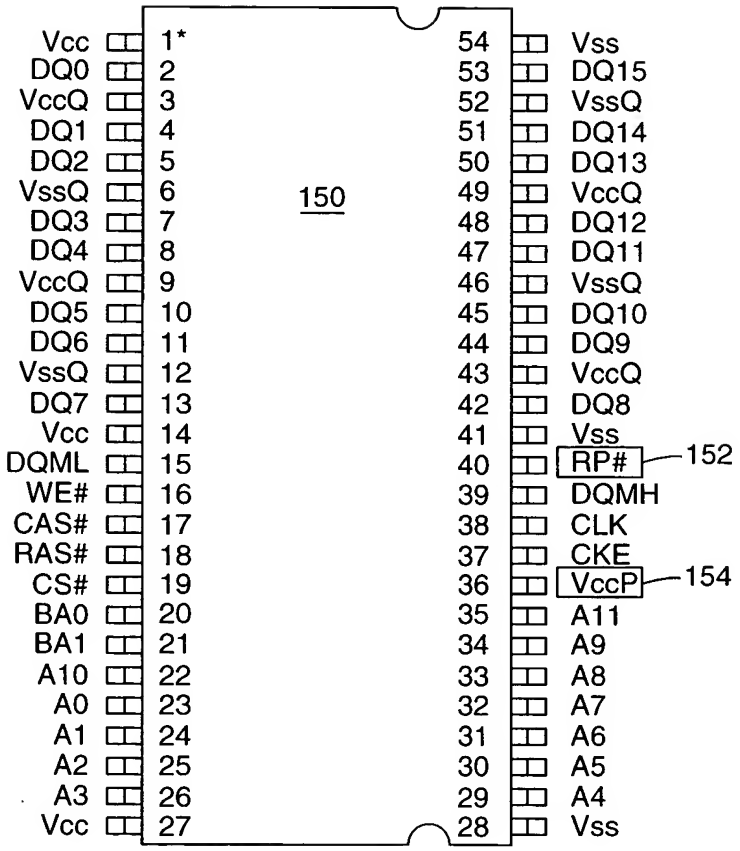

Vcc 1*
DQ0 2
VccQ 3
DQ1 4
DQ2 5
VssQ 6
DQ3 7
DQ4 8
VccQ 9
DQ5 10
DQ6 11
VssQ 12
DQ7 13
Vcc 14
DQML 15
WE# 16
CAS# 17
RAS# 18
CS# 19
BA0 20
BA1 21
A10 22
A0 23
A1 24
A2 25
A3 26
Vcc 27
150
54 Vss
53 DQ15
52 VssQ
51 DQ14
50 DQ13
49 VccQ
48 DQ12
47 DQ11
46 VssQ
45 DQ10
44 DQ9
43 VccQ
42 DQ8
41 Vss
40 RP#
39 DQMH
38 CLK
37 CKE
36 VccP
35 A11
34 A9
33 A8
32 A7
31 A6
30 A5
29 A4
28 Vss
152
154

Fig. 1B

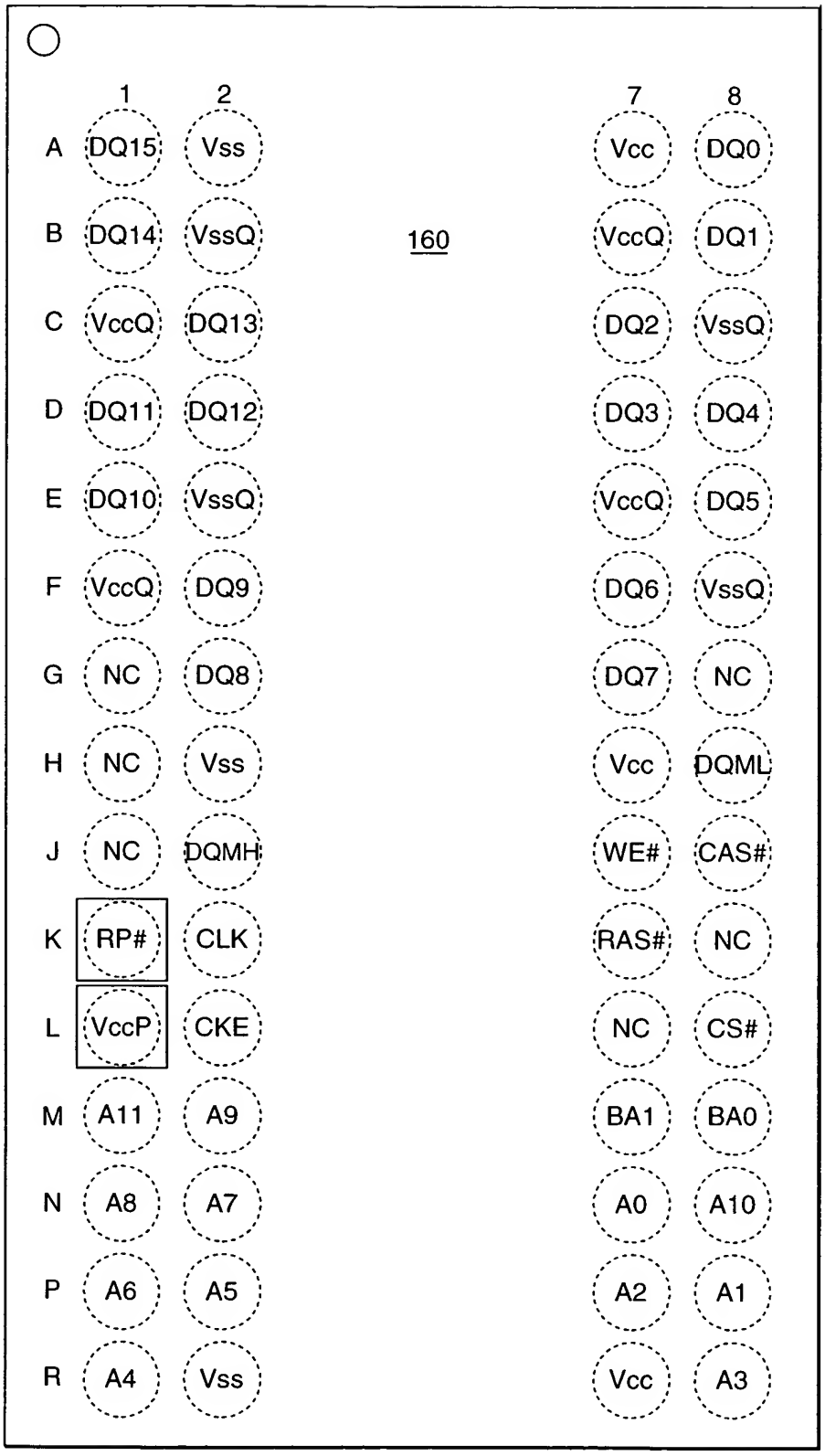

1
2
7
8
A DQ15 Vss Vcc DQ0
B DQ14 VssQ 160 VccQ DQ1
C VccQ DQ13 DQ2 VssQ
D DQ11 DQ12 DQ3 DQ4
E DQ10 VssQ VccQ DQ5
F VccQ DQ9 DQ6 VssQ
G NC DQ8 DQ7 NC
H NC Vss Vcc DQML
J NC DQMH WE# CAS#
K RP# CLK RAS# NC
L VccP CKE NC CS#
M A11 A9 BA1 BA0
N A8 A7 A0 A10
P A6 A5 A2 A1
R A4 Vss Vcc A3

Fig. 1C

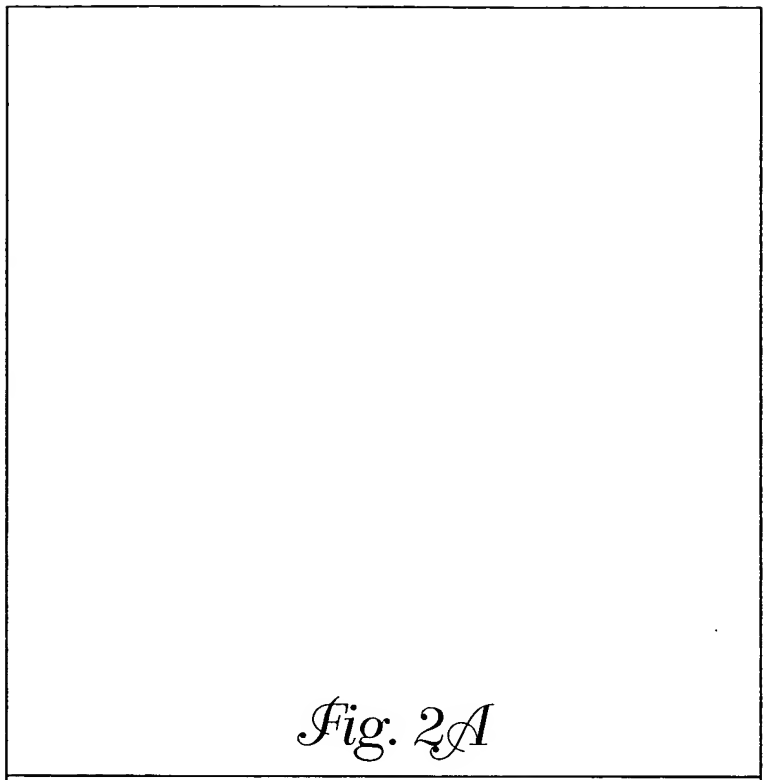


Fig. 2A

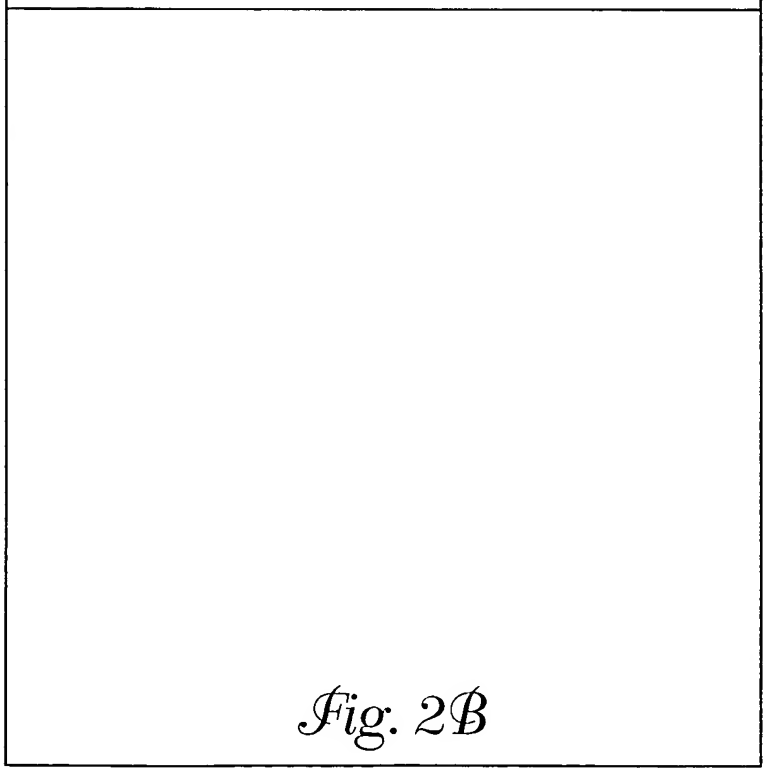


Fig. 2B

Fig. 2

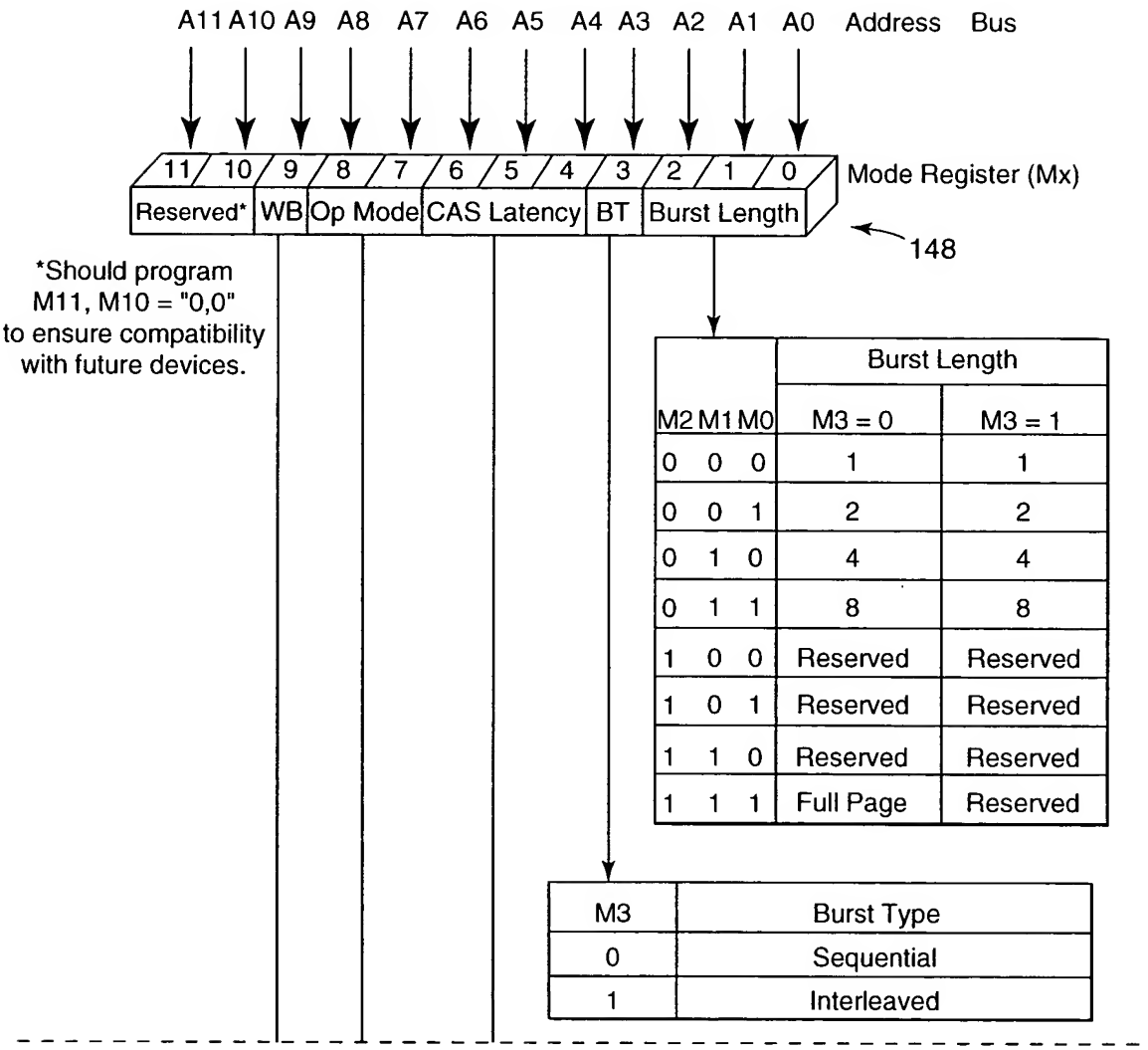
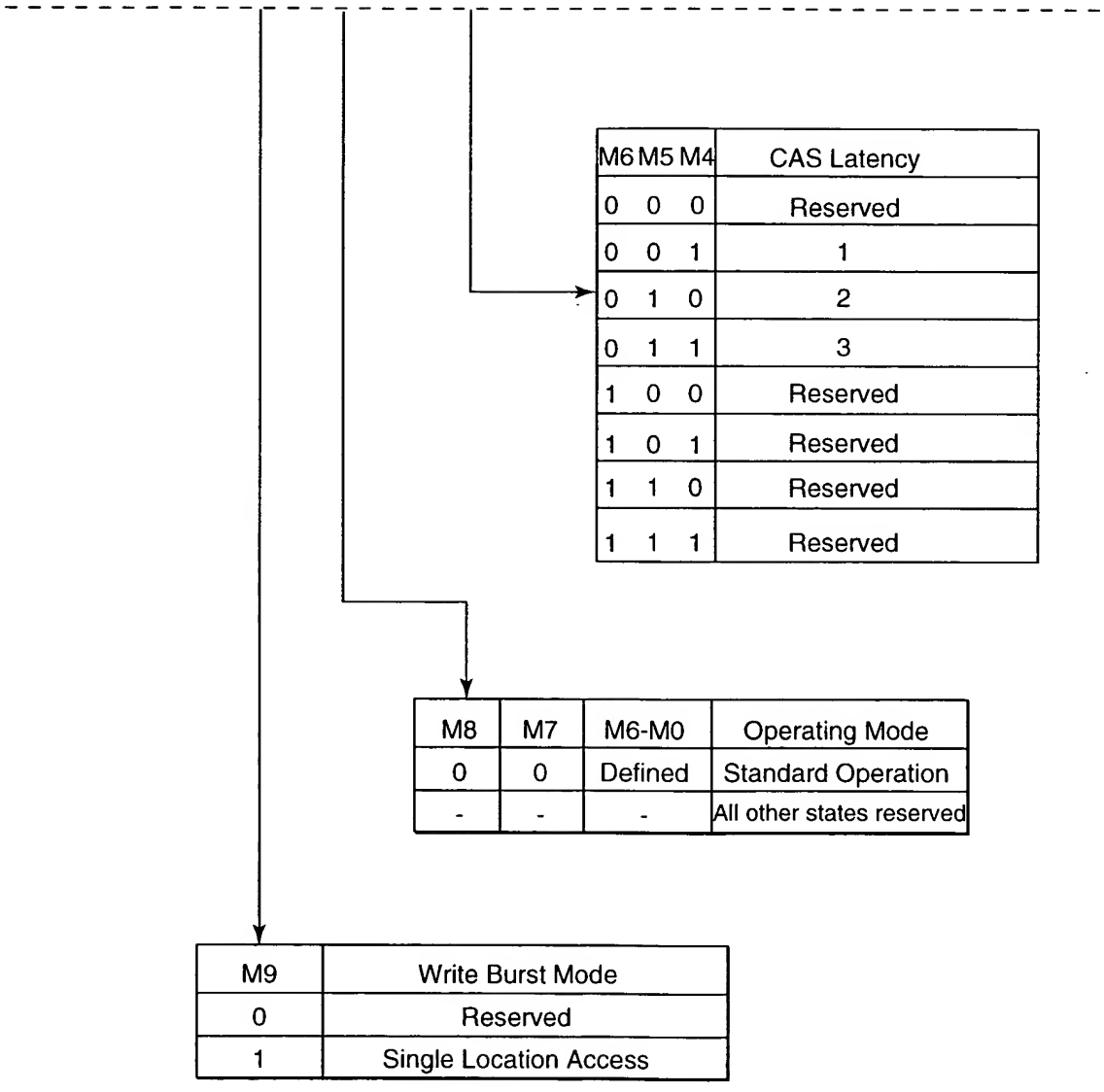

A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 Address Bus
11 10 9 8 7 6 5 4 3 2 1 0
Reserved* WB Op Mode CAS Latency BT Burst Length
Mode Register (Mx)
148
*Should program M11, M10 = "0,0" to ensure compatibility with future devices.
Burst Length
M2 M1 M0 M3 = 0 M3 = 1
0 0 0 1 1
0 0 1 2 2
0 1 0 4 4
0 1 1 8 8
1 0 0 Reserved Reserved
1 0 1 Reserved Reserved
1 1 0 Reserved Reserved
1 1 1 Full Page Reserved
M3 Burst Type
0 Sequential
1 Interleaved

Fig. 2A



M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Reserved
1	Single Location Access

Fig. 2B

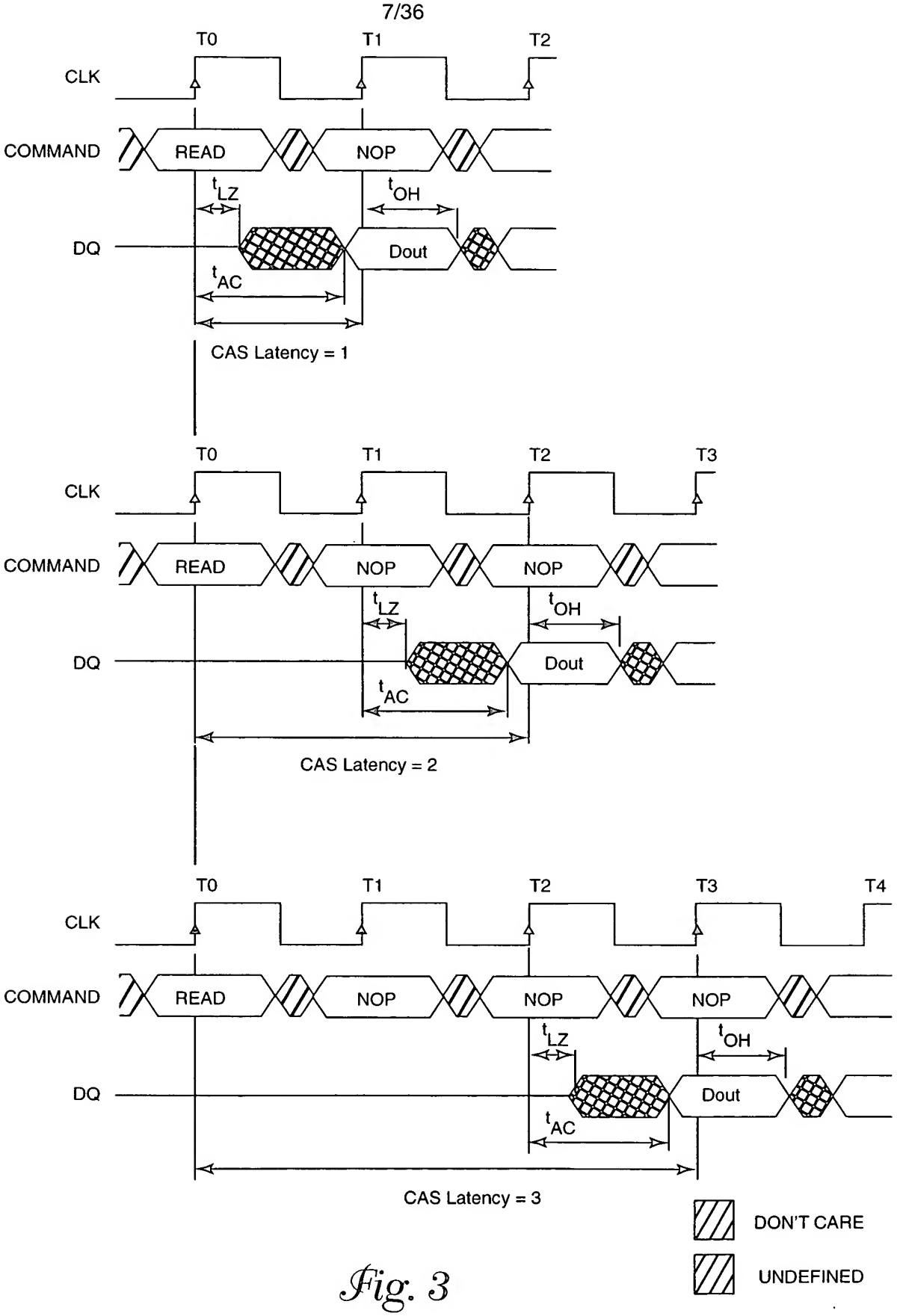

T0
T1
T2
CLK
COMMAND
READ
NOP
t_{LZ}
t_{OH}
DQ
Dout
t_{AC}
CAS Latency = 1
T0
T1
T2
T3
CLK
COMMAND
READ
NOP
NOP
t_{LZ}
t_{OH}
DQ
Dout
t_{AC}
CAS Latency = 2
T0
T1
T2
T3
T4
CLK
COMMAND
READ
NOP
NOP
NOP
t_{LZ}
t_{OH}
DQ
Dout
t_{AC}
CAS Latency = 3
DON'T CARE
UNDEFINED

Fig. 3

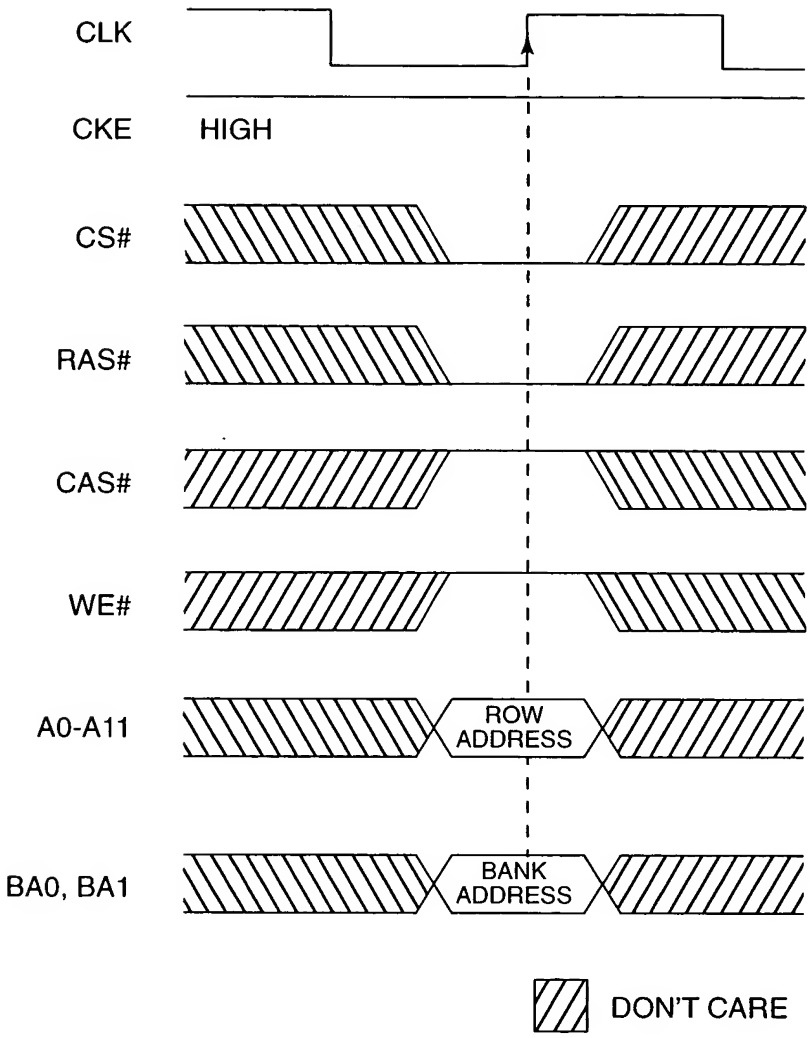

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A11
ROW ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 4

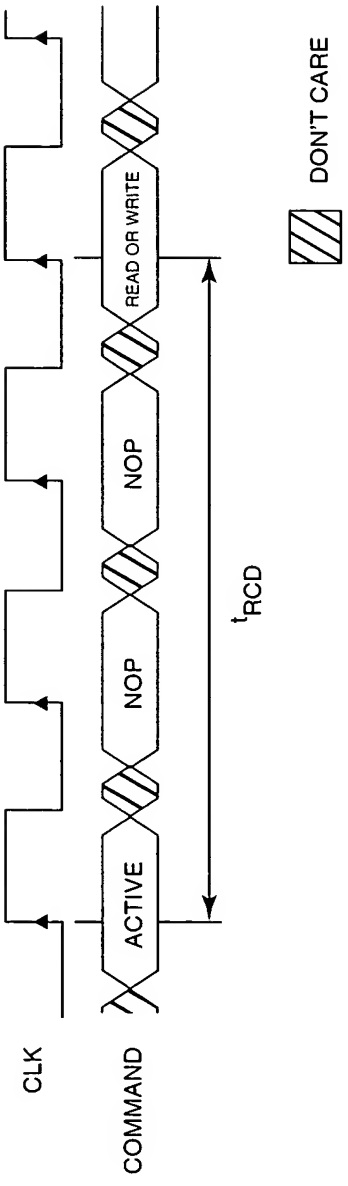

T0
T1
T2
T3
T4
CLK
COMMAND
ACTIVE
NOP
NOP
READ OR WRITE
t_{RCD}
DON'T CARE

Fig. 5

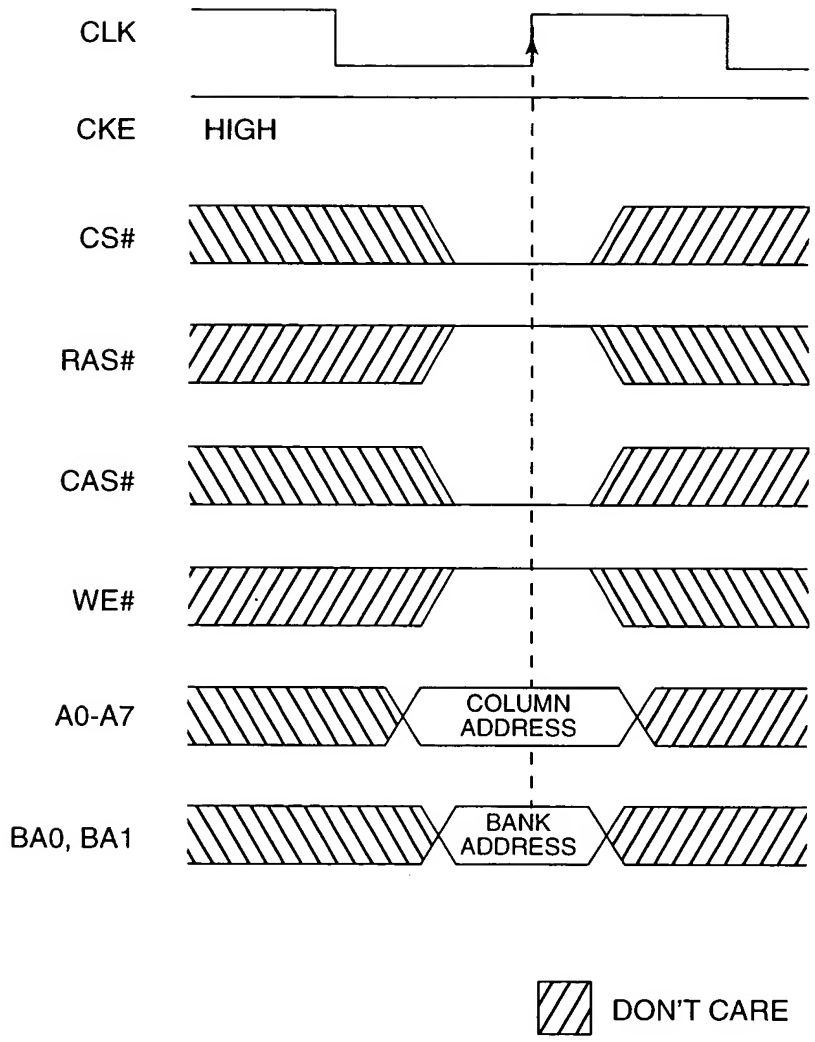
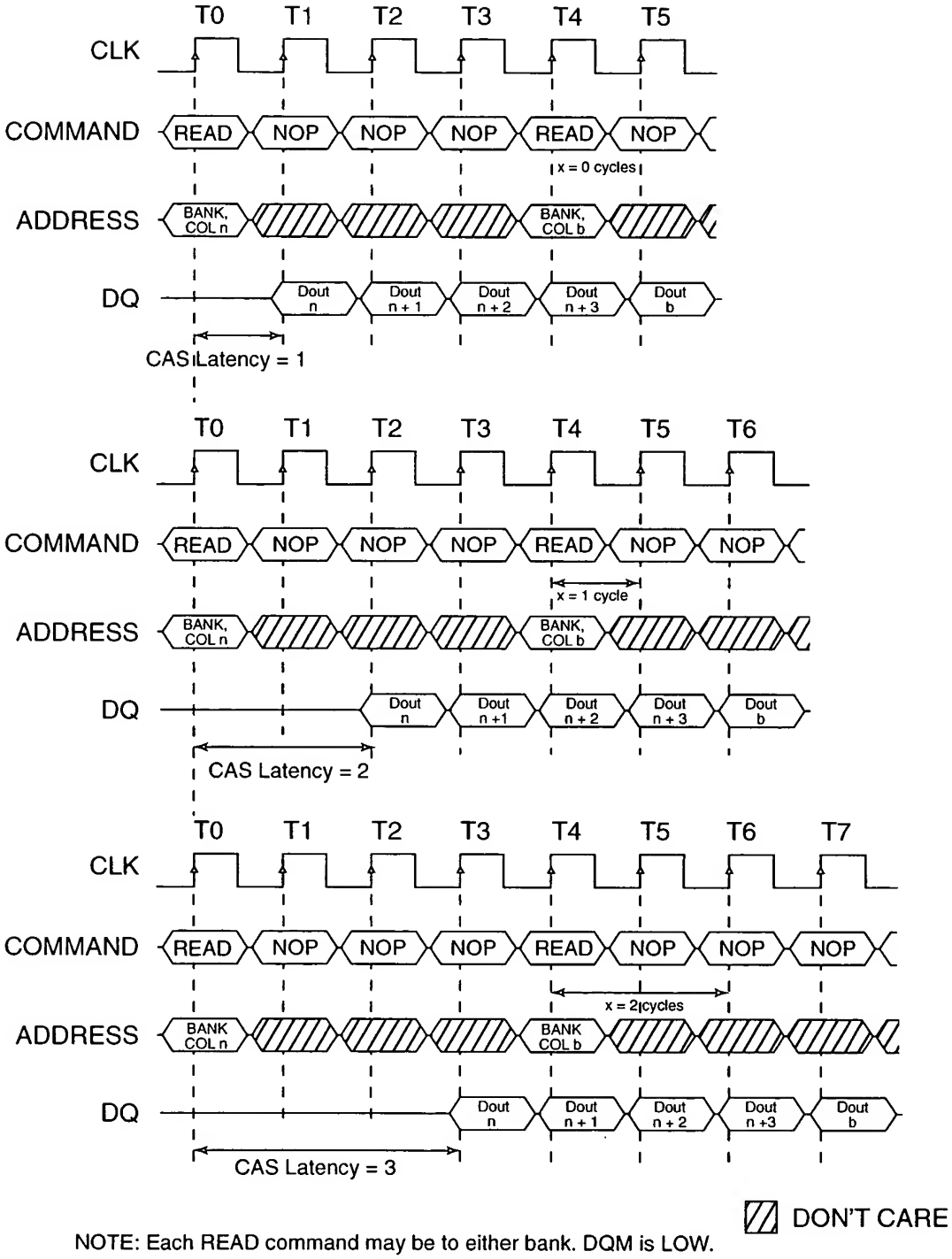
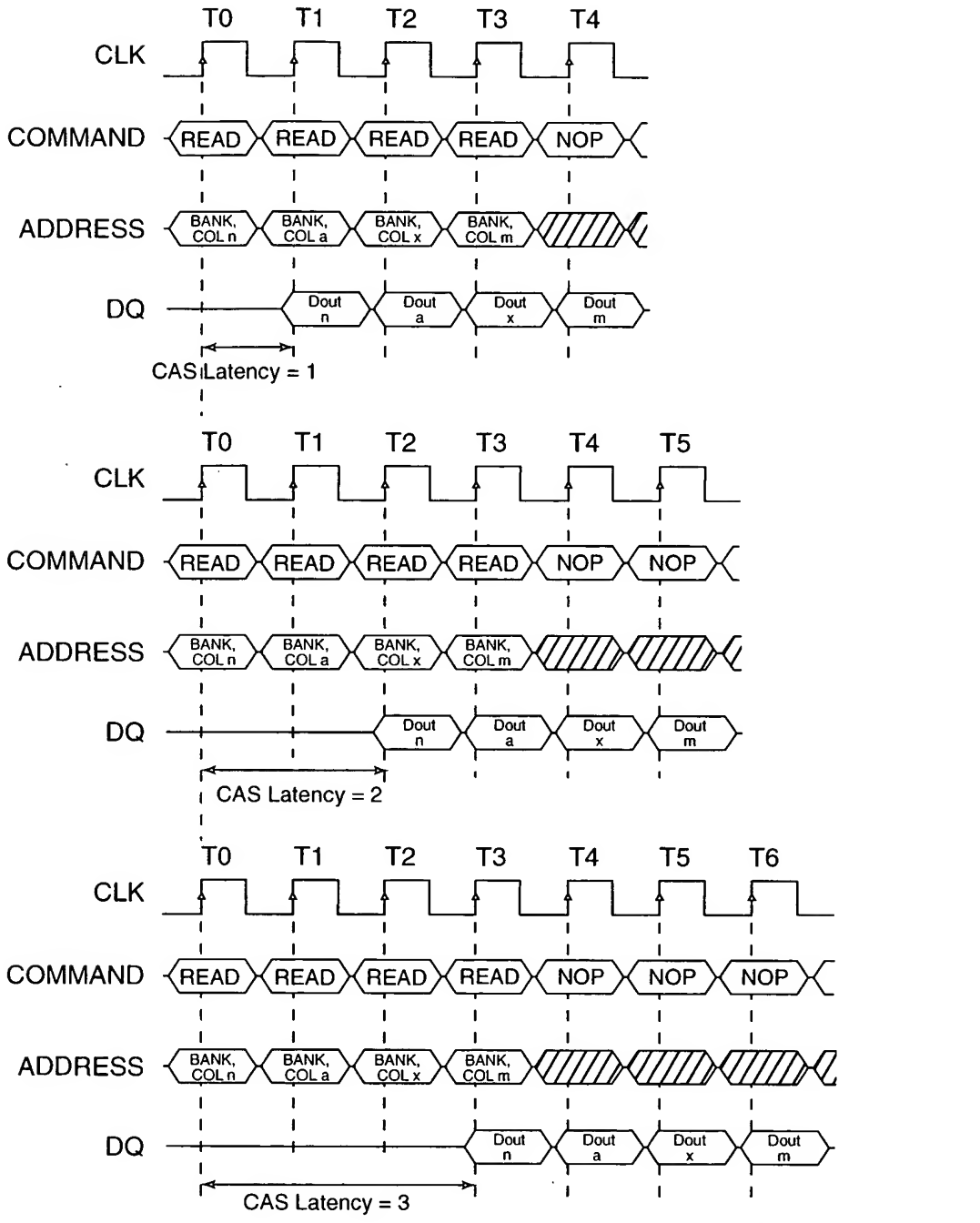

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A7
COLUMN ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 6



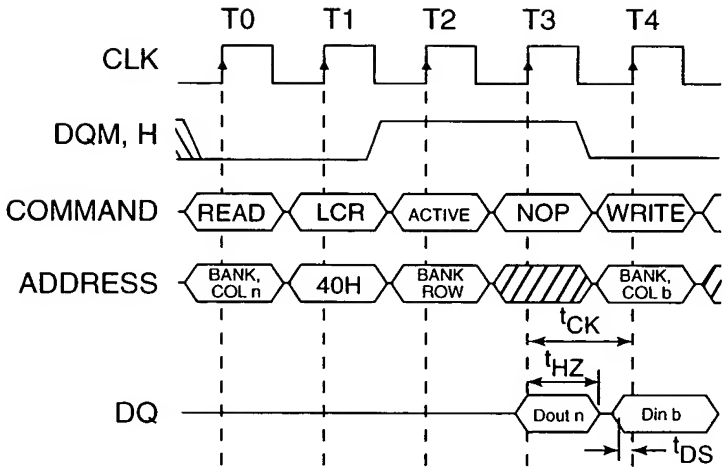
NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 7



NOTE: Each READ command may be to either bank. DQM is LOW.

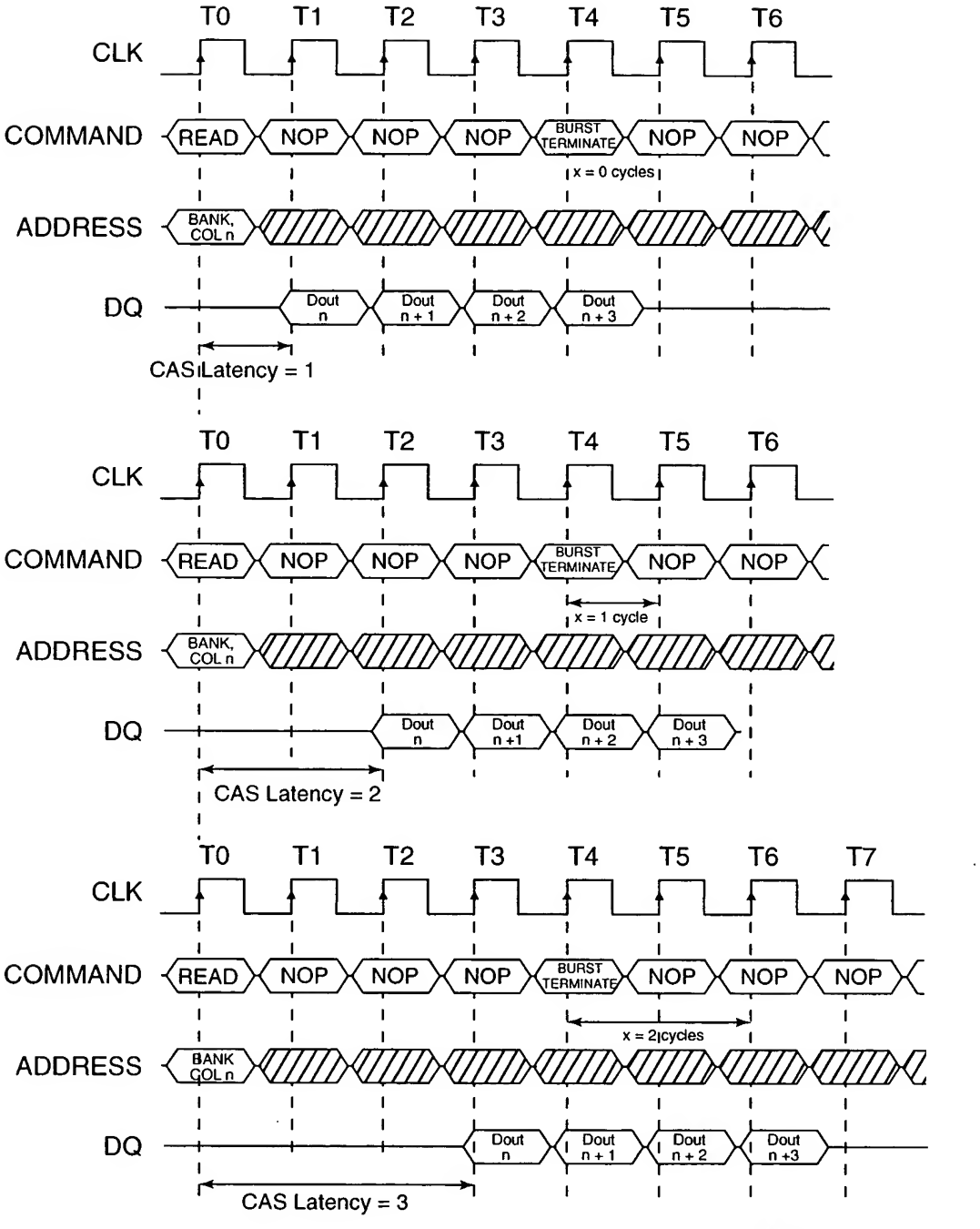
Fig. 8



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

▨ DON'T CARE

Fig. 9



NOTE: DQM is LOW.

Fig. 10

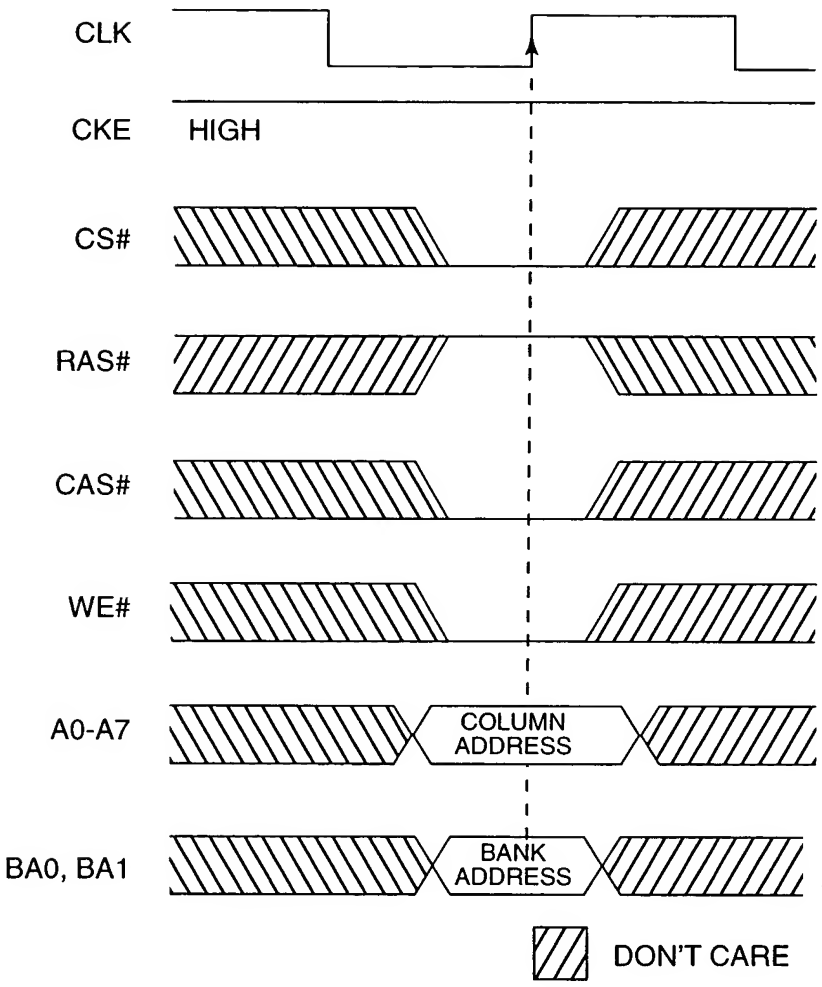
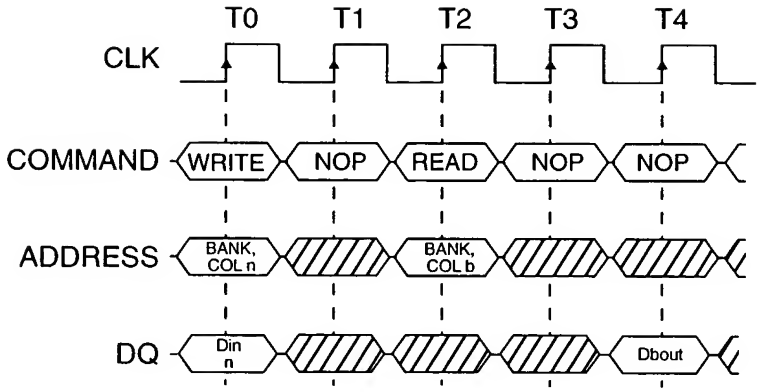

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A7
COLUMN ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 11



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data. For more details, refer to Truth Tables 4 and 5.

DON'T CARE

Fig. 12

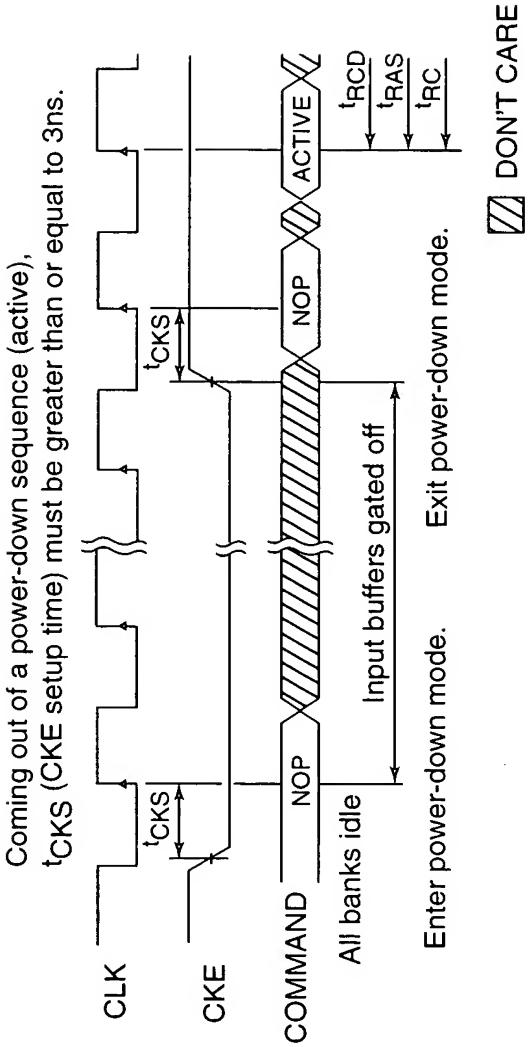
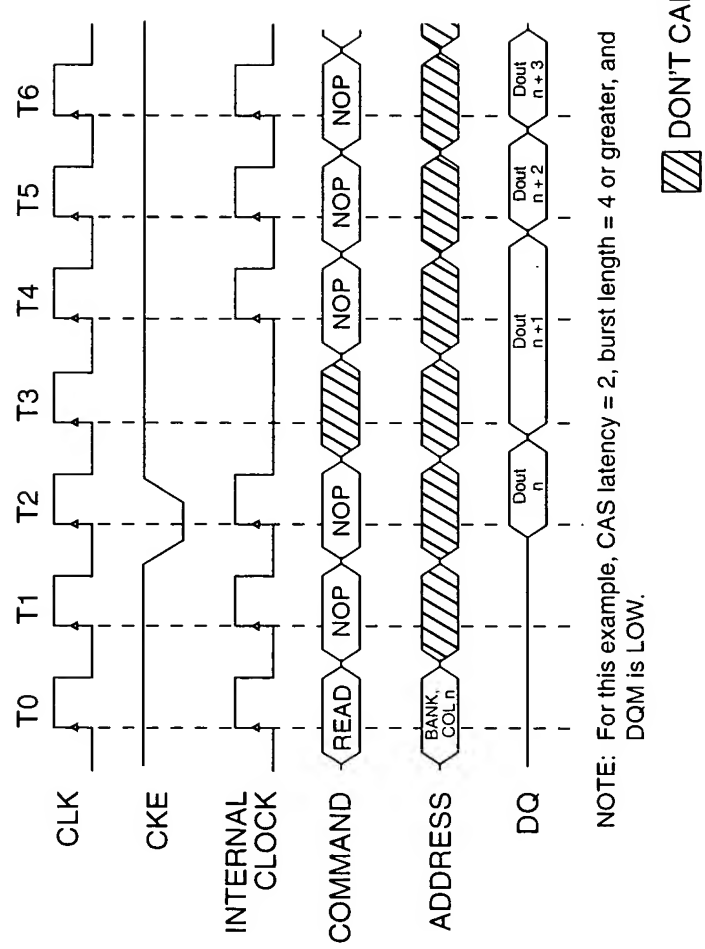
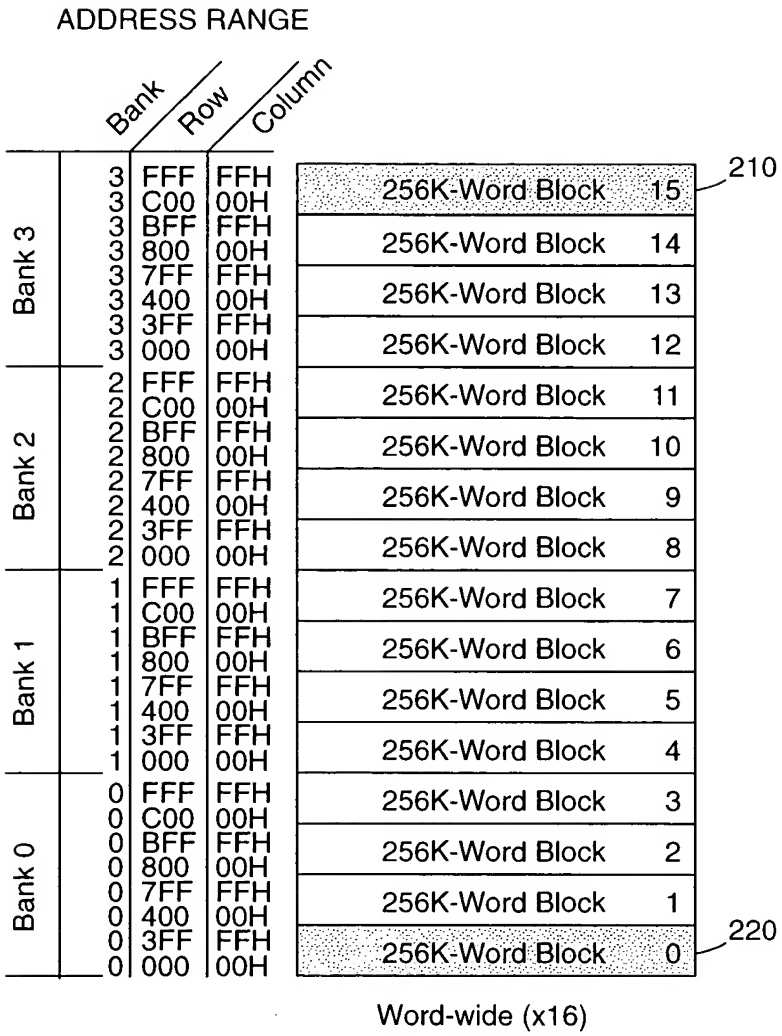

Coming out of a power-down sequence (active),
tCKS (CKE setup time) must be greater than or equal to 3ns.
CLK
CKE
COMMAND
tCKS
tCKS
NOP
NOP
ACTIVE
tRCD
tRAS
tRC
All banks idle
Input buffers gated off
Enter power-down mode.
Exit power-down mode.
DON'T CARE

Fig. 13



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, and DQM is LOW.

Fig. 14



See BLOCK PROTECT/UNPROTECT SEQUENCE for detailed information.

Fig. 15

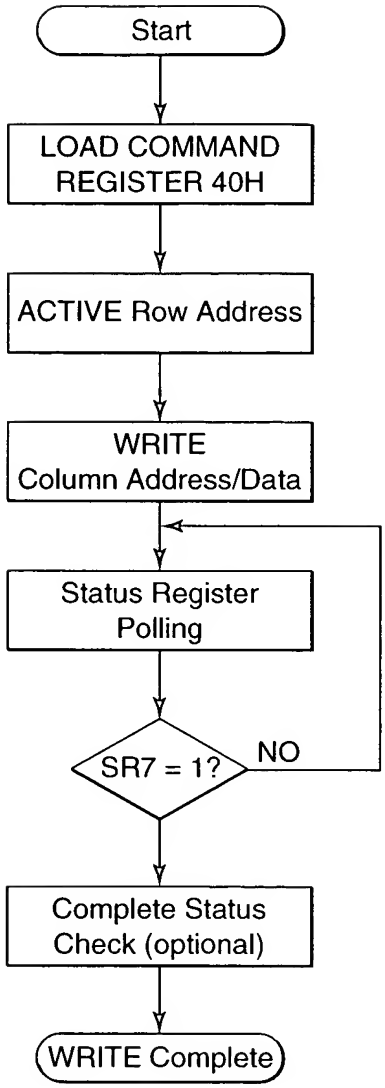

Start
LOAD COMMAND REGISTER 40H
ACTIVE Row Address
WRITE Column Address/Data
Status Register Polling
SR7 = 1?
NO
Complete Status Check (optional)
WRITE Complete

Fig. 16

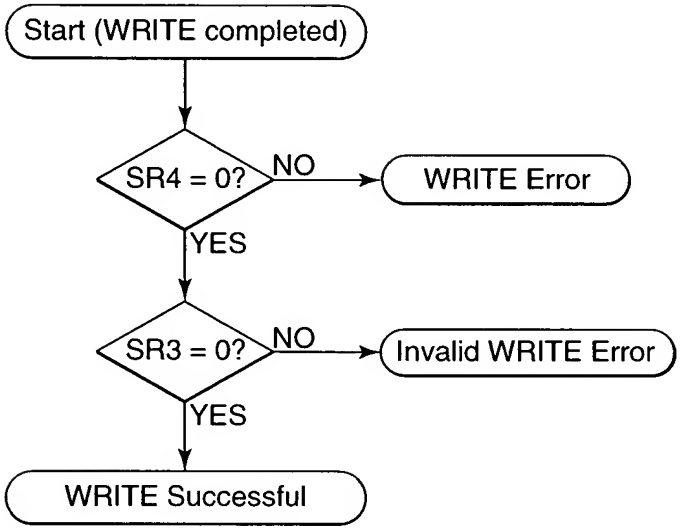

Start (WRITE completed)
SR4 = 0?
NO
WRITE Error
YES
SR3 = 0?
NO
Invalid WRITE Error
YES
WRITE Successful

Fig. 17

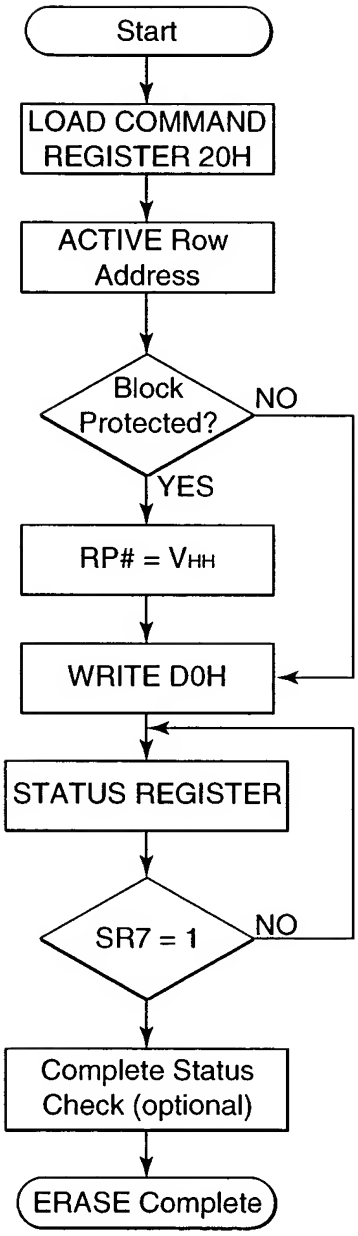

Start
LOAD COMMAND REGISTER 20H
ACTIVE Row Address
Block Protected?
NO
YES
RP# = VHH
WRITE D0H
STATUS REGISTER
SR7 = 1
NO
Complete Status Check (optional)
ERASE Complete

Fig. 18

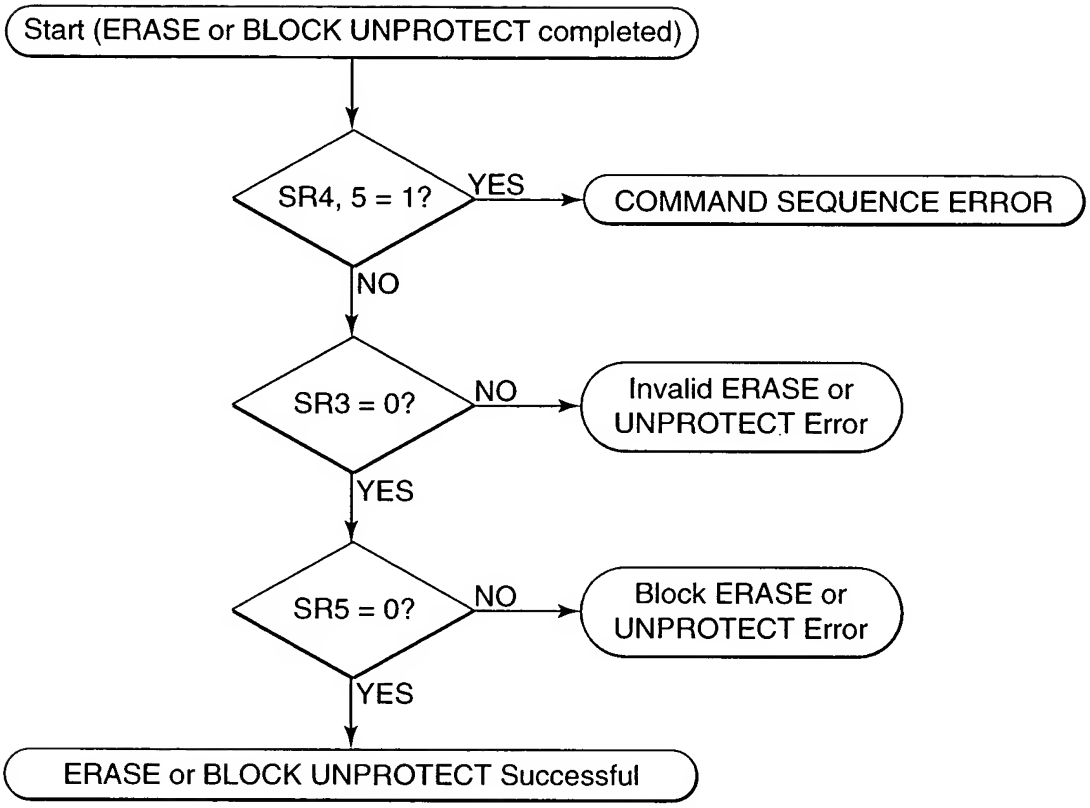

Start (ERASE or BLOCK UNPROTECT completed)
SR4, 5 = 1?
YES
COMMAND SEQUENCE ERROR
NO
SR3 = 0?
NO
Invalid ERASE or UNPROTECT Error
YES
SR5 = 0?
NO
Block ERASE or UNPROTECT Error
YES
ERASE or BLOCK UNPROTECT Successful

Fig. 19

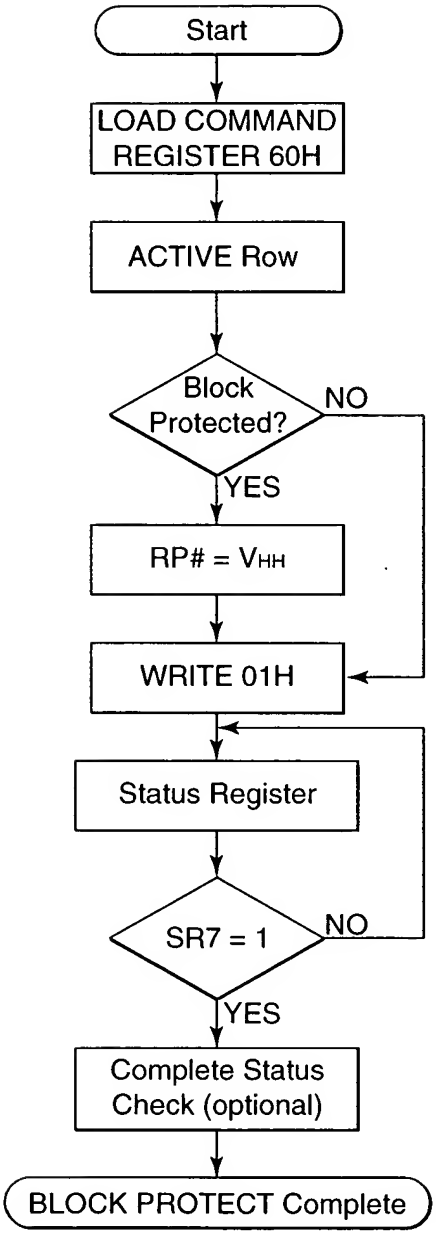

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
Block Protected?
NO
YES
RP# = VHH
WRITE 01H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
BLOCK PROTECT Complete

Fig. 20

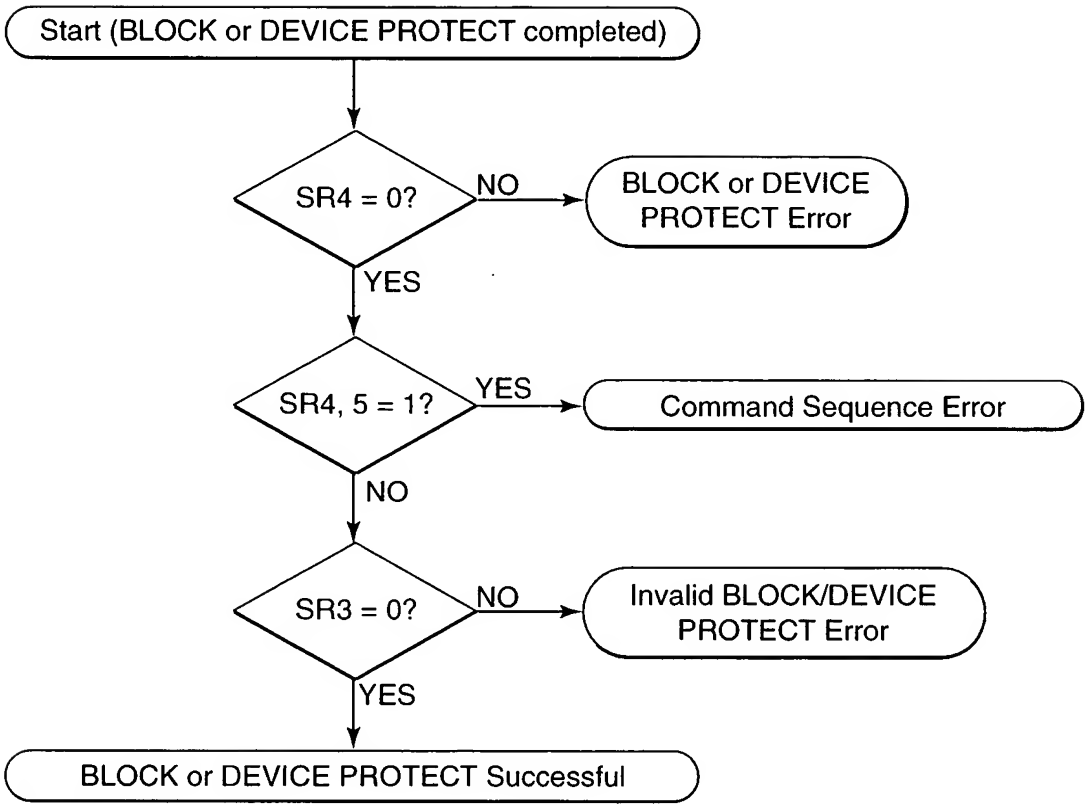

Start (BLOCK or DEVICE PROTECT completed)
SR4 = 0?
NO
BLOCK or DEVICE PROTECT Error
YES
SR4, 5 = 1?
YES
Command Sequence Error
NO
SR3 = 0?
NO
Invalid BLOCK/DEVICE PROTECT Error
YES
BLOCK or DEVICE PROTECT Successful

Fig. 21

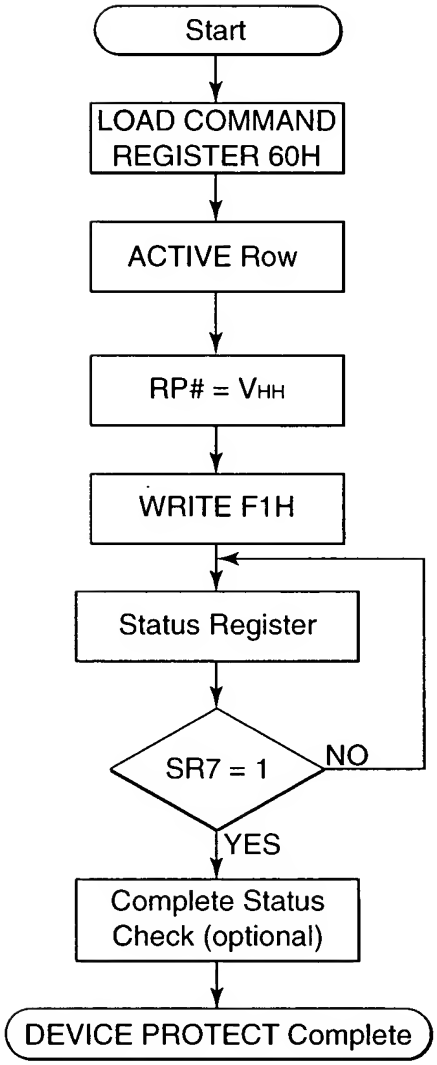

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
RP# = VHH
WRITE F1H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
DEVICE PROTECT Complete

Fig. 22

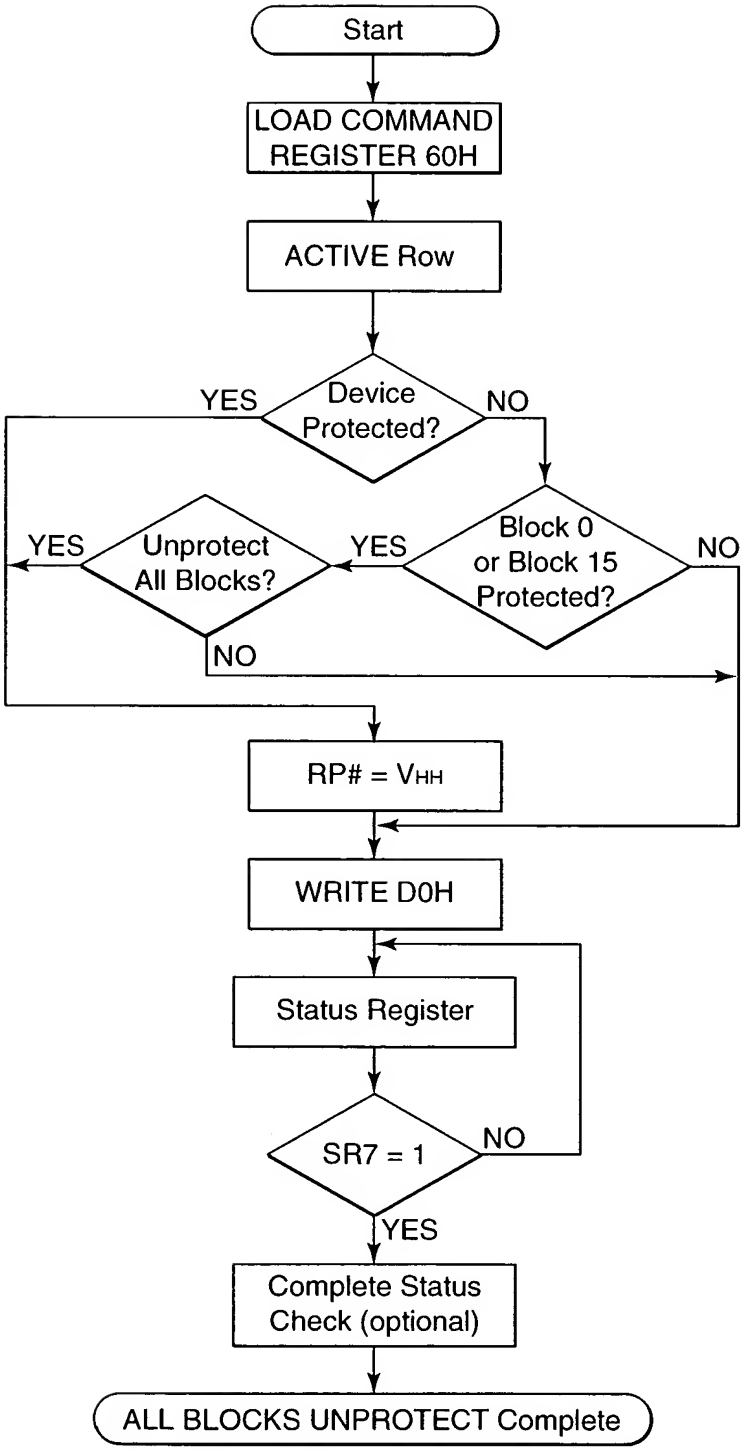

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
Device Protected?
YES
NO
Unprotect All Blocks?
YES
NO
Block 0 or Block 15 Protected?
YES
NO
RP# = VHH
WRITE D0H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
ALL BLOCKS UNPROTECT Complete

Fig. 23

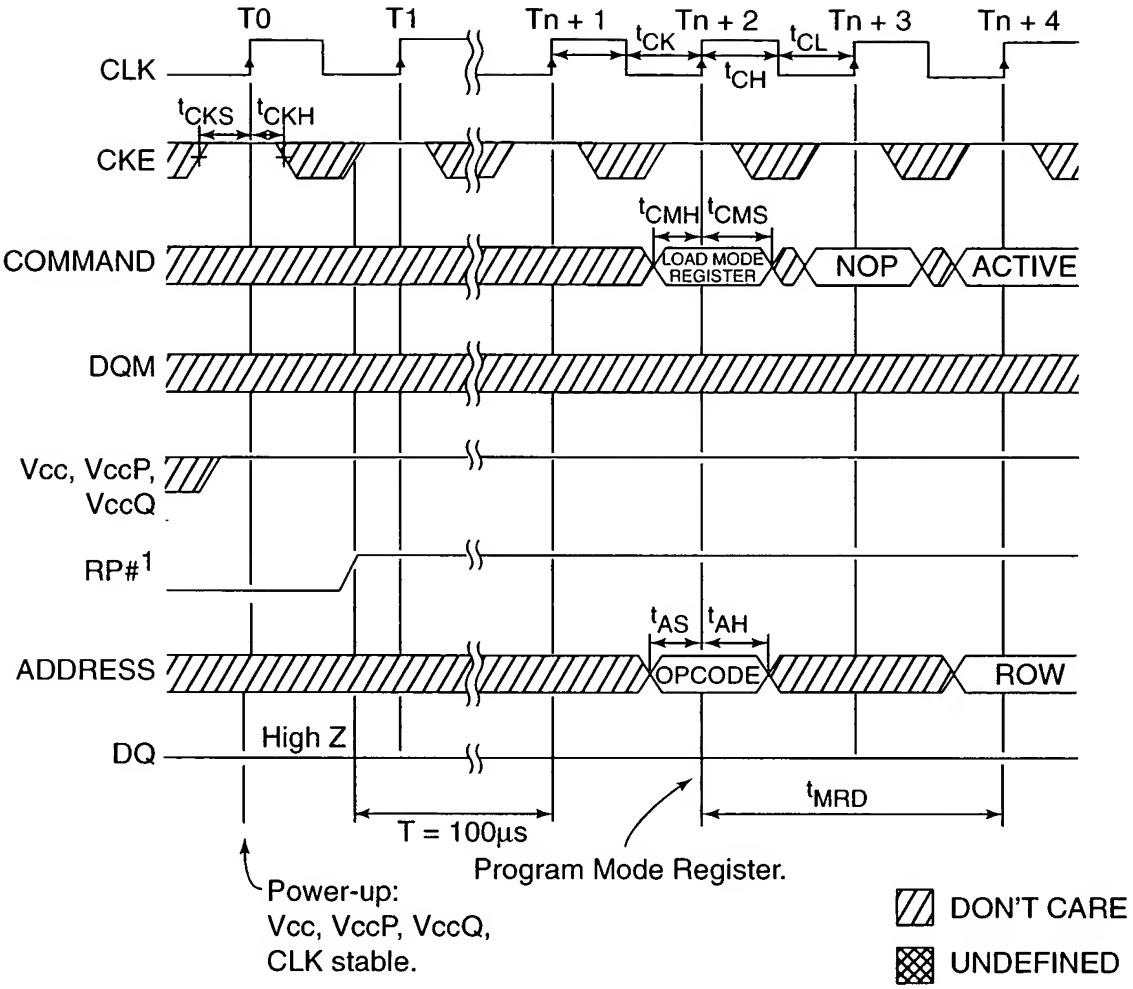

T0
T1
Tn + 1
Tn + 2
Tn + 3
Tn + 4
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMH
tCMS
COMMAND
LOAD MODE REGISTER
NOP
ACTIVE
DQM
Vcc, VccP, VccQ
RP#1
tAS
tAH
ADDRESS
OPCODE
ROW
DQ
High Z
tMRD
T = 100µs
Program Mode Register.
Power-up:
Vcc, VccP, VccQ,
CLK stable.
DON'T CARE
UNDEFINED

Fig. 24

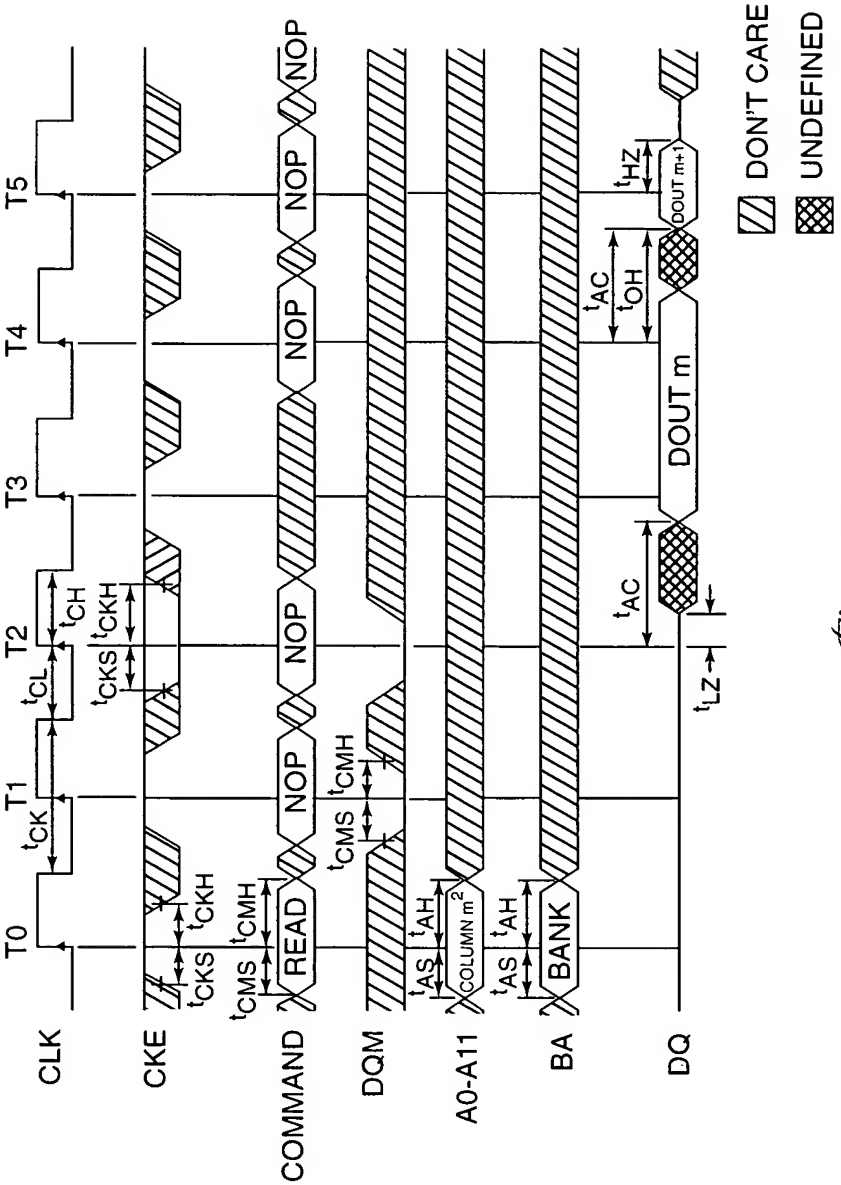

T0
T1
T2
T3
T4
T5
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
READ
NOP
BANK
COLUMN m
DOUT m
DOUT m+1
tCK
tCL
tCH
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tAC
tOH
tHZ
tLZ
DON'T CARE
UNDEFINED

Fig. 25

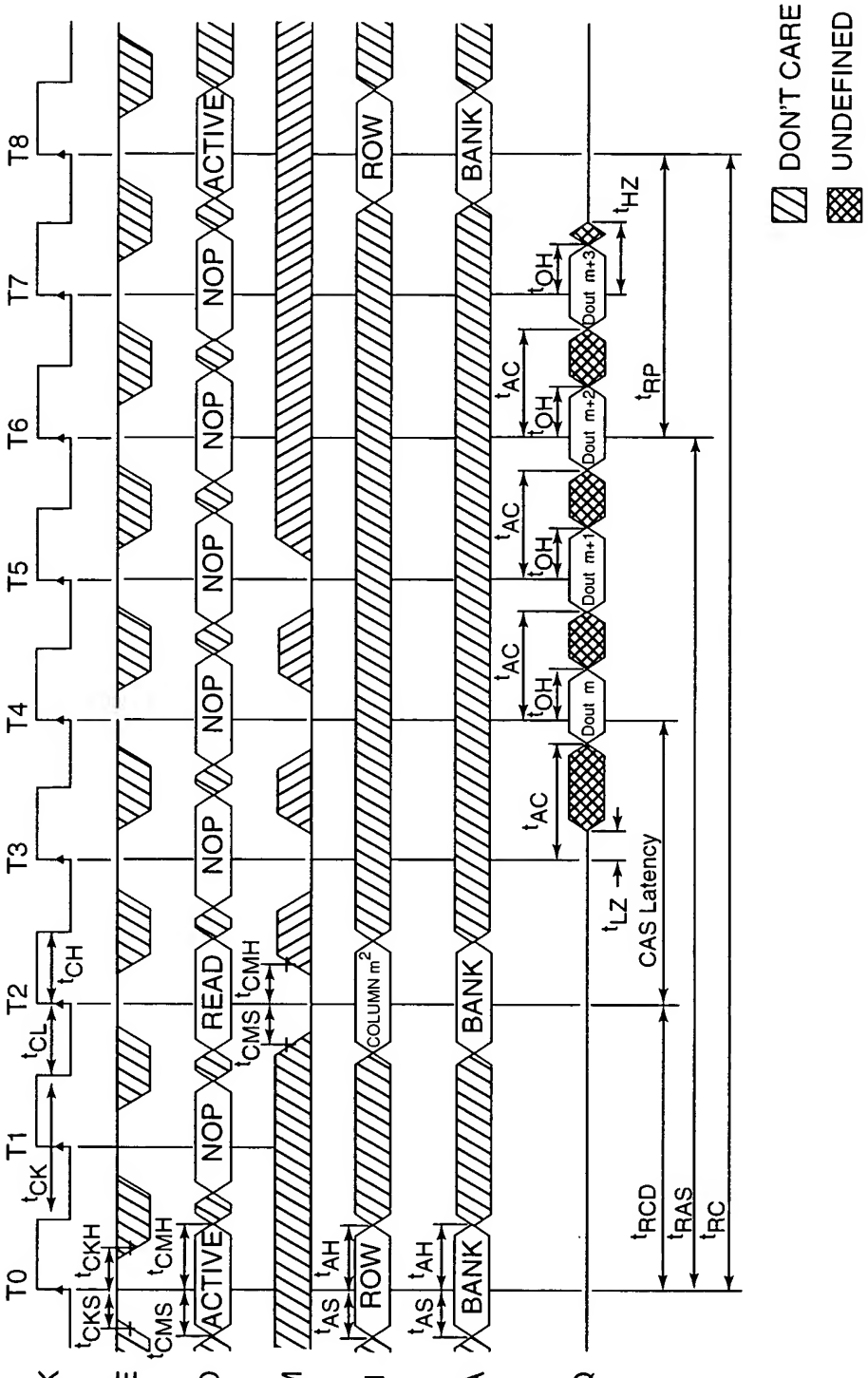

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
ACTIVE
NOP
READ
BANK
ROW
COLUMN m
Dout m
Dout m+1
Dout m+2
Dout m+3
tCK
tCH
tCL
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tAC
tOH
tHZ
tLZ
tRP
tRCD
tRAS
tRC
CAS Latency
DON'T CARE
UNDEFINED

Fig. 26

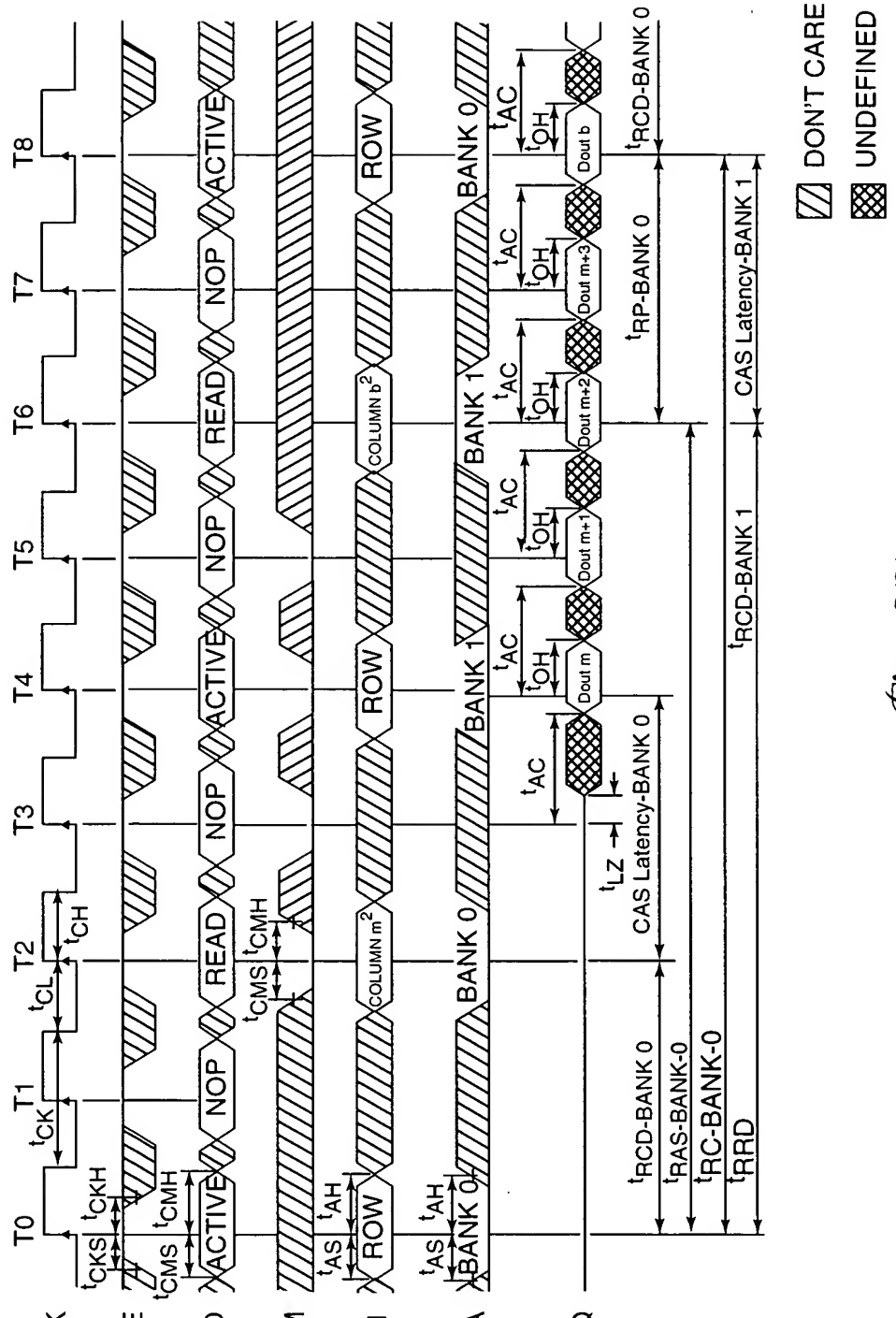

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
ACTIVE
NOP
READ
ROW
COLUMN m
COLUMN b
BANK 0
BANK 1
Dout m
Dout m+1
Dout m+2
Dout m+3
Dout b
tCK
tCKS
tCKH
tCL
tCH
tCMS
tCMH
tAS
tAH
tAC
tOH
tLZ
tRCD-BANK 0
tRAS-BANK-0
tRC-BANK-0
tRRD
tRCD-BANK 1
tRP-BANK 0
CAS Latency-BANK 0
CAS Latency-BANK 1
DON'T CARE
UNDEFINED

Fig. 27

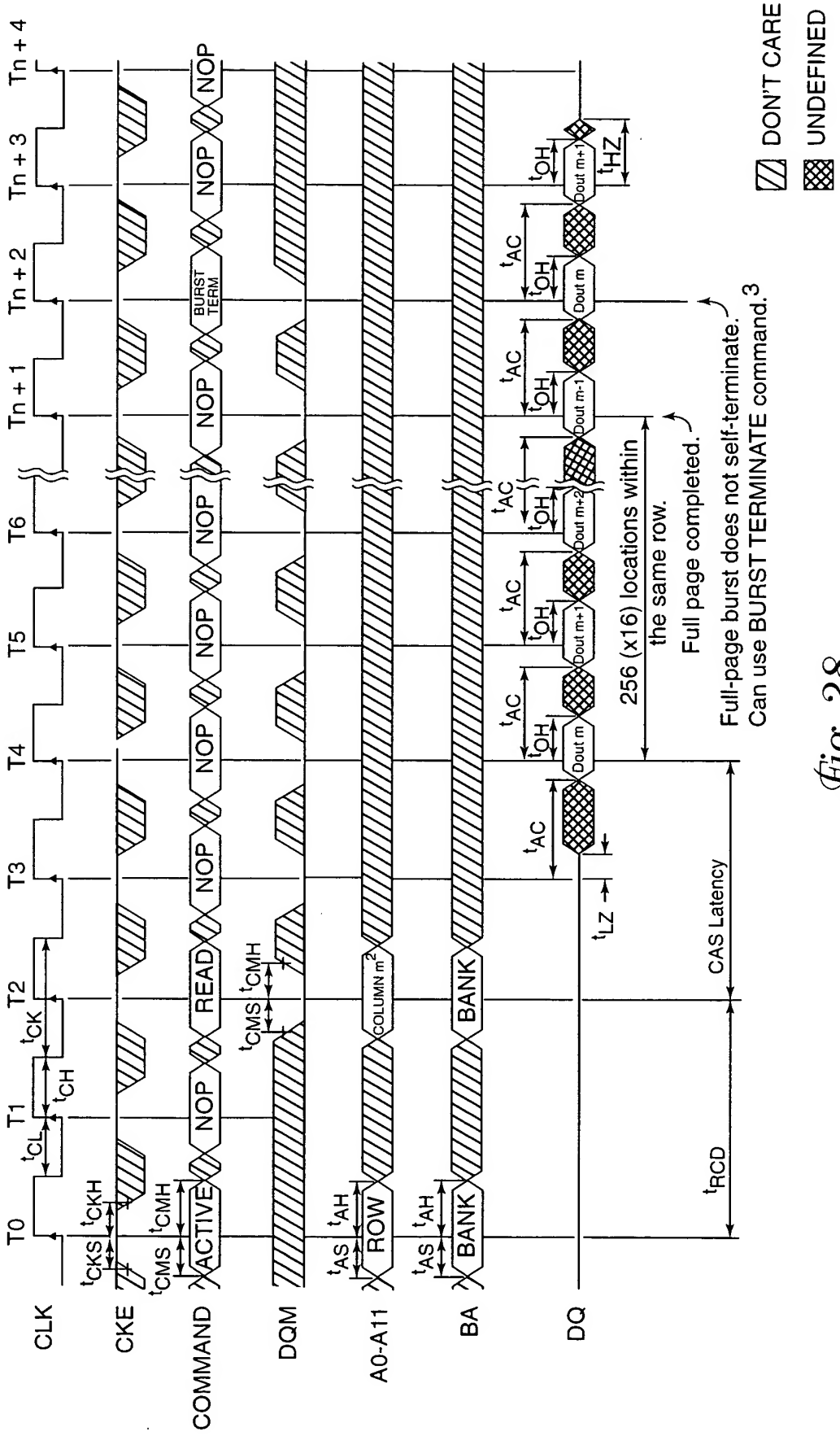

T0
T1
T2
T3
T4
T5
T6
Tn + 1
Tn + 2
Tn + 3
Tn + 4
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
ACTIVE
READ
NOP
BURST TERM
ROW
COLUMN m
BANK
Dout m
Dout m+1
Dout m+2
Dout m-1
Dout m
Dout m+1
tCL
tCH
tCK
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tAC
tOH
tLZ
tHZ
tRCD
CAS Latency
256 (x16) locations within the same row.
Full page completed.
Full-page burst does not self-terminate.
Can use BURST TERMINATE command.3
DON'T CARE
UNDEFINED

Fig. 28

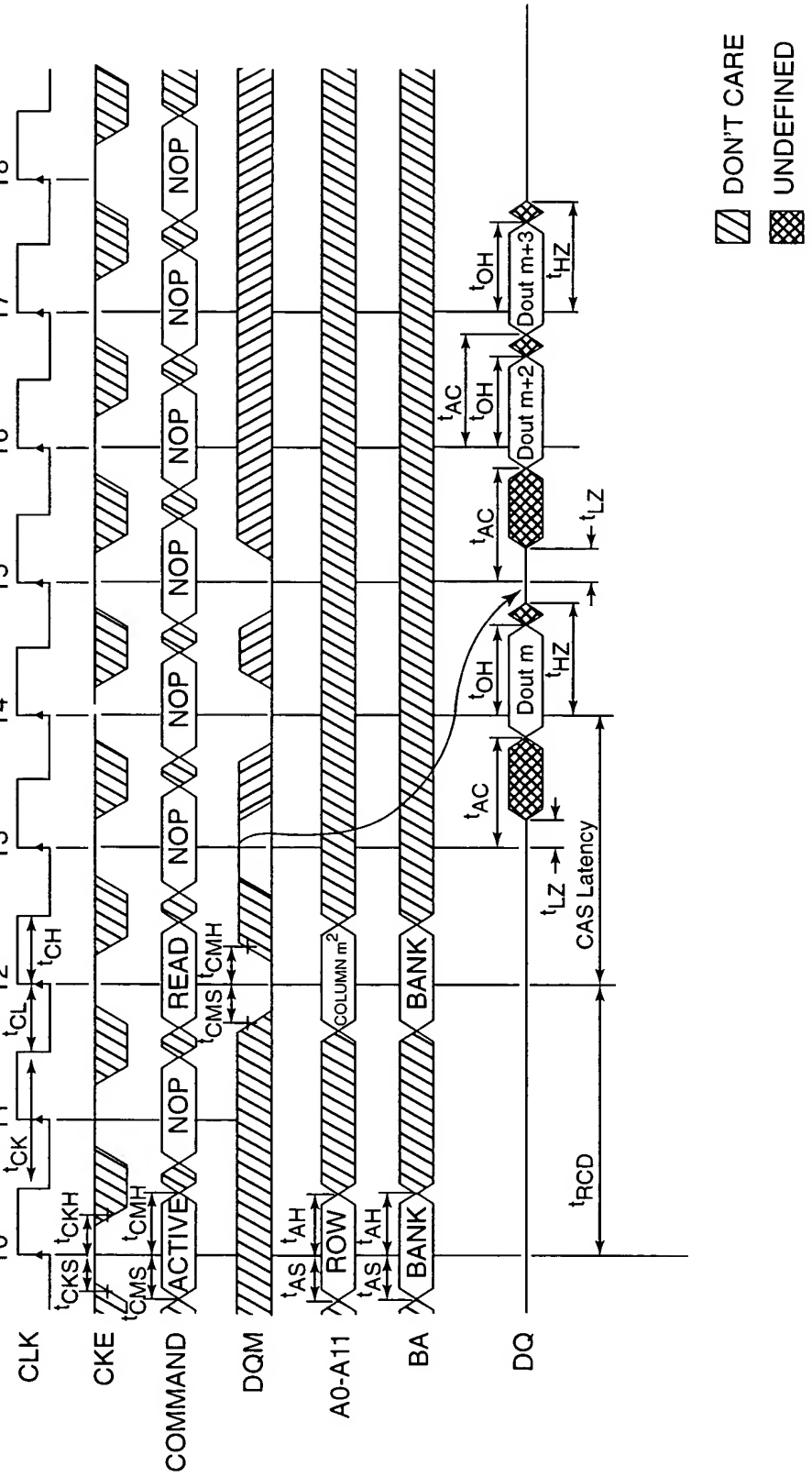

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
ACTIVE
NOP
READ
ROW
COLUMN m
BANK
Dout m
Dout m+2
Dout m+3
CAS Latency
DON'T CARE
UNDEFINED

Fig. 29

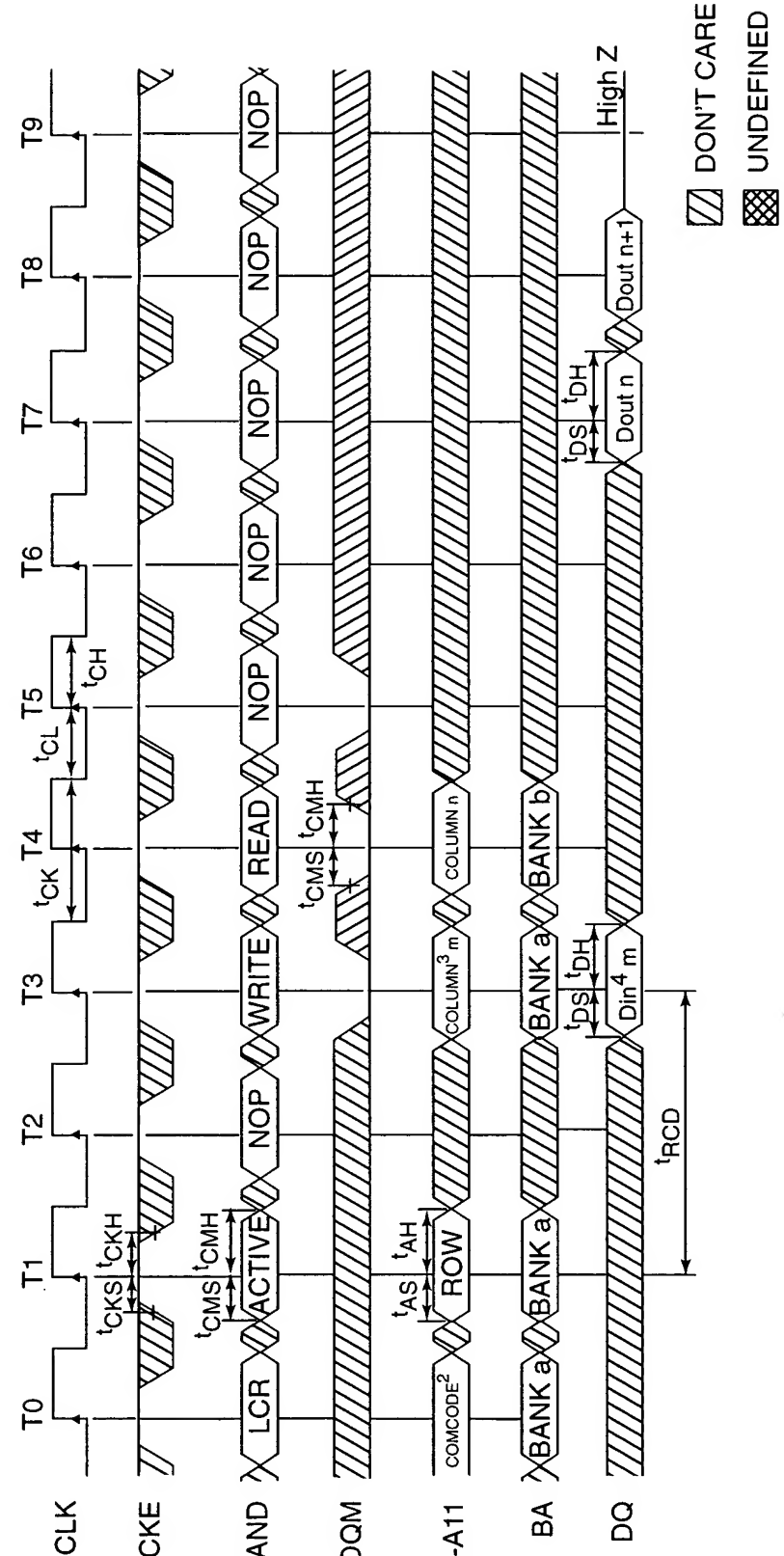

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
LCR
ACTIVE
NOP
WRITE
READ
COMCODE2
ROW
COLUMN3 m
COLUMN n
BANK a
BANK b
Din4 m
Dout n
Dout n+1
High Z
tCKS
tCKH
tCMS
tCMH
tCK
tCL
tCH
tAS
tAH
tDS
tDH
tRCD
DON'T CARE
UNDEFINED

Fig. 30

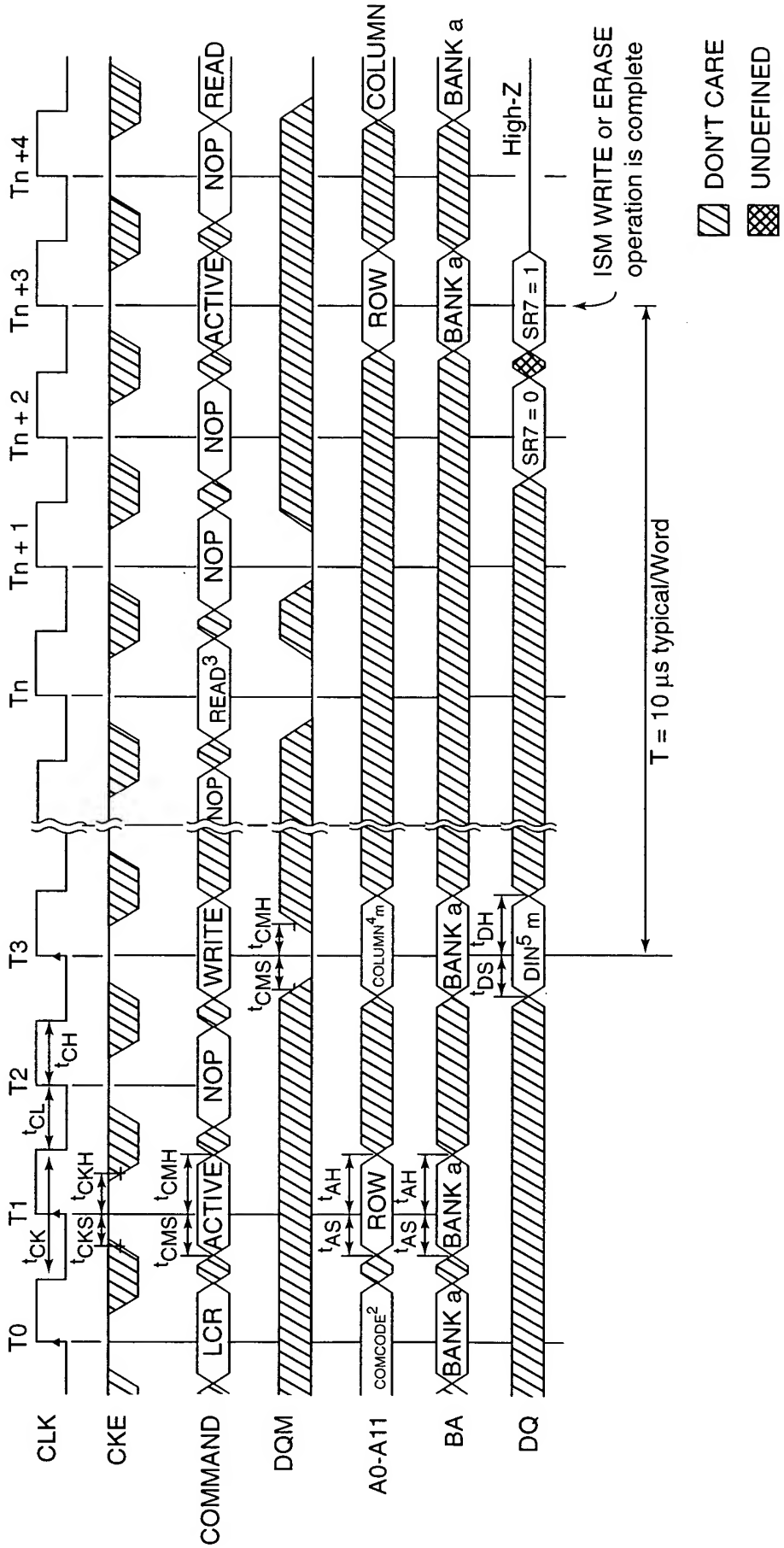

T0
T1
T2
T3
Tn
Tn + 1
Tn + 2
Tn + 3
Tn +4
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
LCR
ACTIVE
NOP
WRITE
READ3
NOP
NOP
ACTIVE
NOP
READ
COMCODE2
ROW
COLUMN4 m
ROW
COLUMN
BANK a
BANK a
BANK a
BANK a
BANK a
High-Z
DIN5 m
SR7 = 0
SR7 = 1
tCK
tCKS
tCKH
tCL
tCH
tCMS
tCMH
tAS
tAH
tDS
tDH
T = 10 µs typical/Word
ISM WRITE or ERASE operation is complete
DON'T CARE
UNDEFINED

Fig. 31

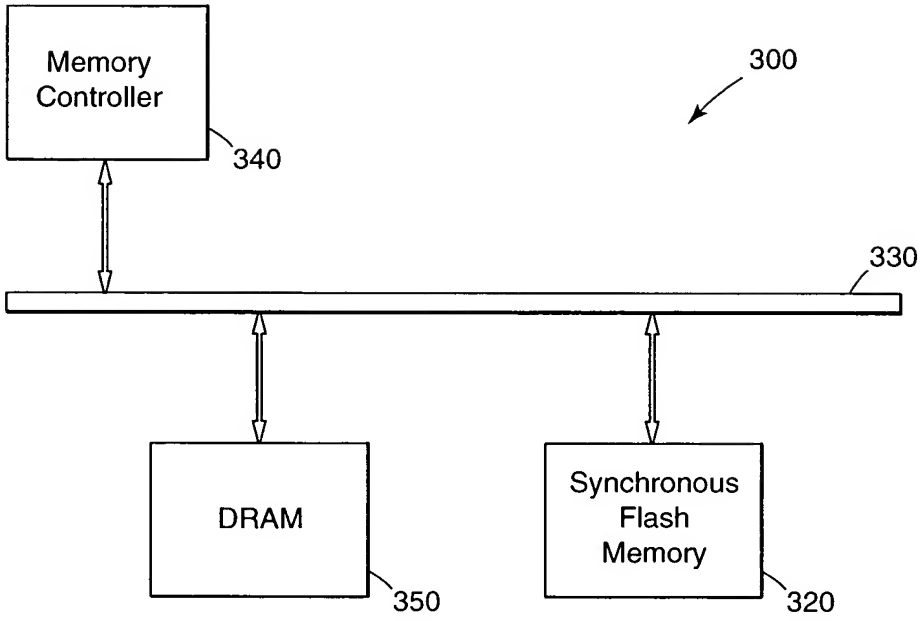

Memory Controller
340
300
330
DRAM
350
Synchronous Flash Memory
320

Fig. 32